Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.057”**

**PAD FUNCTION:**

1. **V+**
2. **N/C**
3. **S16**
4. **S15**
5. **S14**
6. **S13**
7. **S12**
8. **S11**
9. **S10**
10. **S9**
11. **GND**
12. **A3**
13. **A2**
14. **A1**
15. **A0**
16. **EN**
17. **S1**
18. **S2**
19. **S3**
20. **S4**
21. **S5**
22. **S6**
23. **S7**
24. **S8**
25. **V-**
26. **D**

**2 1 26**

**25**

**24**

**23**

**22**

**21**

**20**

**19**

**18**

**17**

**3**

**4**

**5**

**6**

**7**

**8**

**9**

**10**

**11**

**12 13 14 15 16**

**A**

**CSIZ**

**MASK**

**REF**

**.111”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size = .003 x .003”**

**Backside Potential: V+**

**Mask Ref: CSIZ A**

**APPROVED BY: DK DIE SIZE .057” X .111” DATE: 9/23/21**

**MFG: SILICONIX THICKNESS .009” P/N: DG506B**

**DG 10.1.2**

#### Rev B, 7/1